Field Tests of a New High-Speed Pattern Recognition Trigger for Ground-Based Gamma-Ray Telescope Arrays

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***Abstract*–We have developed a three-stage, high-speed trigger for use in an array of imaging atmospheric Cherenkov telescopes (IACTs), which are used for the study of cosmic high-energy gamma-ray sources. This trigger has the ability to recognize patterns of Cherenkov light generated by gamma-ray initiated air showers in the atmosphere and correlate these patterns across multiple telescopes in the IACT array to form a stereoscopic real-time pattern recognition trigger. New hardware and firmware sampling at 400MHz with programmable coincidence recognition timing and programmable delay compensation over 500 pixel channels in an IACT camera has been produced which generates triggers from the coincidence of any three adjacent pixels within the camera. Reduction of the required coincidence time to 5 ns and the concomitant reduction in dead time from the faster logic allow operation at lower discriminator thresholds relative to existing systems, enabling studies of lower energy gamma-ray events. A successful field test of the first two stages of this pattern recognition hardware has been performed on one of the IACTs of the VERITAS array located in Southern Arizona. We present the results of these tests and compare them to the performance of the existing VERITAS trigger system. A subsequent field test where hardware is connected to multiple VERITAS telescopes to exercise the stereoscopic features is in the planning stages.**

I. Introduction

We have designed a fast topological trigger system [1], [4] with the goal of reducing the energy threshold for detection of gamma rays by a factor of two below the threshold of current imaging atmospheric-Cherenkov telescopes (IACTs) around 130 GeV. In its full implementation this trigger will enable the real-time analysis of trigger-maps across an array of telescopes and thereby improve the rejection of background over the current generation of trigger systems. Aspects that ultimately determine how low the energy threshold can be set include not only the speed and sophistication of the trigger, but also the memory depth in the front-end electronics and the speed of the data acquisition system. This topological trigger may be part of a VERITAS upgrade proposal [2] or it may interface with a highly integrated camera on next generation IACTs, such as the Advanced Gamma-Ray Imaging System (AGIS).

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The overall design of this system has been presented in detail in earlier publications [1], [2], [3] so only a short summary of the overall system is provided herein. This paper concentrates upon tests of a subset of the hardware connected to one of four telescopes of the VERITAS array. Features of the system that were exercised in this field test include

1. Capability of the system to trigger upon specific pixel patterns as specified;
2. Ability of the system to connect to the existing telescope electronics and run in parallel with, and without adversely affecting, scheduled observations;
3. Ability of the system to compensate for timing variations on a per-pixel basis;
4. Demonstration of built-in diagnostic features; and
5. Demonstration of complete operation at 400MHz sampling rate resulting in a 5 ns coincidence width.

The Imaging Air Cherenkov Telescope (IACT) technique used by VERITAS and other experiments is based upon the observation that gamma rays entering the atmosphere from astronomical sources generate particle showers that then create very short pulses of Cherenkov light as shown in Fig. 1.

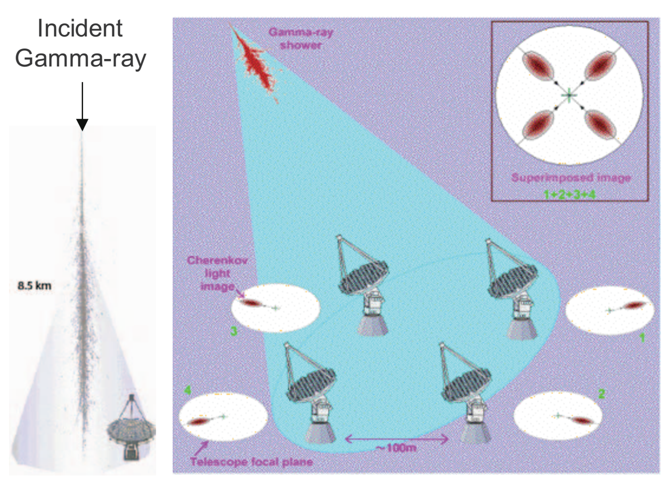

Fig. 1. Illustration of IACT technique. A single gamma-ray shower may result in photons arriving at multiple telescopes simultaneously. Pictures courtesy of VERITAS[5].

Each telescope face is an array of mirrors that reflect the light from the Cherenkov shower onto an array of photomultiplier tubes. The outputs of the photomultipliers are connected to fast discriminators (Level 1 of the trigger) resulting in a bit pattern indicative of pixels with light input above threshold at any given moment. Differentiation of gamma-ray events from other light-producing events (e.g. cosmic rays, muons or night sky background) is accomplished by imposing the requirements that

1. Multiple adjacent pixels must be illuminated at the same time (filters out random singles from background) and
2. The total number of pixels illuminated when coincidence occurs must be sufficiently small and the area of coincidence be sufficiently compact (filters out cosmic ray and muon events).

As shown in Fig. 2, events from differing interactions are visually quite distinct.

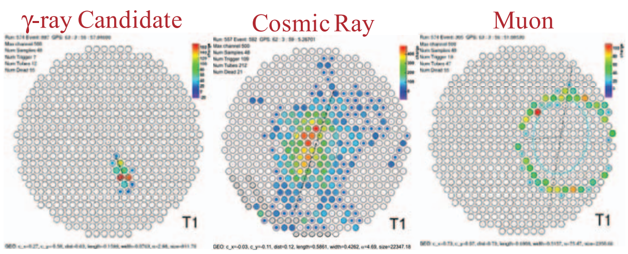

Fig. 2. Example pixel illumination patterns from various interaction types. Pictures courtesy of VERITAS.

II. Description of the Trigger System

The topological trigger system uses a modular approach in which I/O cards are used to tap into the existing cable plant of the telescope and connect to pixel bits. The number of bits is too large for practical connection to a single FPGA or single board so the telescope face is subdivided logically into regions. Each region has its own "L1.5" processor board that performs the coincidence algorithm upon the entire region plus an overlap range of pixels that are also driven to the L1.5 board of the adjacent region, as shown in Fig. 3.

In the specific case of the VERITAS experiment this results in three L1.5 boards subdividing the 499 pixels of one telescope into regions of ~180 pixels each, but this modular approach is easily adapted to telescopes of any size.

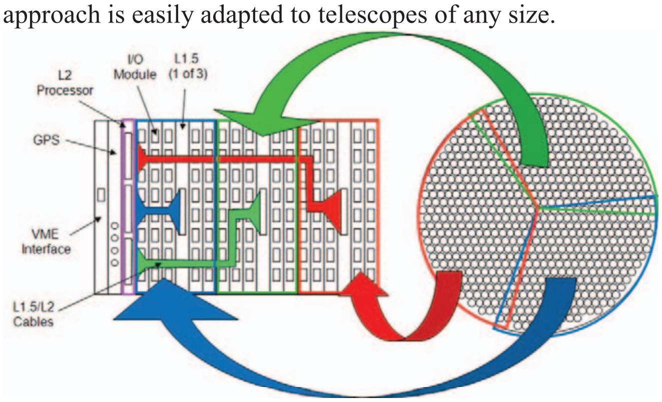

Fig. 3. The pixels of the telescope face are received by I/O cards and mapped into regions. Each region is serviced by its own region processor. Pixels at the boundaries between regions are duplicated to insure no gaps in the logic.

The I/O cards receive, buffer and retransmit the pixel data to the appropriate L1.5 cards over a custom backplane in which each pixel is a unique differential pair transmission line. Signal fidelity and timing is protected by the use of LVDS interconnections, attention to high-speed printed circuit design rules and the use of connectors designed for fast rise time signals. An "L2" processor provides clock distribution and control signals to insure that all L1.5 cards are synchronized and have identical timestamps, as shown in Fig. 4.

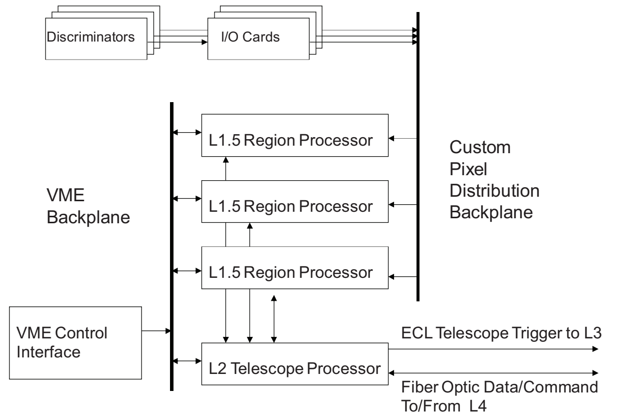

Fig. 4. System block diagram sketch showing relationship between telescope discriminators, L1.5 region trigger processor and L2 telescope processor.

The region processed by each L1.5 card is subdivided into many 7-pixel sub-regions consisting of a center pixel plus the surrounding 6, as shown in Fig. 5. All of the sub-regions in each L1.5 card are simultaneously sampled. If any sub-region has a coincidence the L1.5 card reports the list of all pixels involved in it to the L2.

The L2 asserts a front panel output upon the receipt of any data from any L1.5 for connection to a multi-telescope array trigger (L3). Additionally the L2 collects the data from all L1.5s, merges data with sufficiently close timestamps and calculates the moments (n, Σx, Σy, Σx^2, Σy^2, Σxy) of the resulting data set. This data set is then sent over a fiber optic cable to an "L4 board" that uses the information from multiple L2s to further filter false triggers by calculating the parallax width of the projected position of the shower from all reporting telescopes [6]. In this field test only one telescope was instrumented and therefore the L4 board with the parallax width algorithm could not be tested. We hope to report upon test of this hardware at a later conference after a future test where multiple telescopes are used.

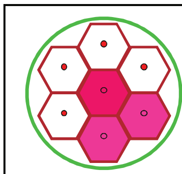

Fig. 5. 3-fold coincidence; center plus any two of the surrounding 6.

III. TEST STAND SETUP AND MEASUREMENTS

A test stand was developed at Argonne to verify the operation and timing of the overall system prior to the field test. Test pixel patterns are generated using a number of LeCroy 1607 CAMAC ECL output register modules. These modules are enabled by a common NIM signal distributed using a fan-out and equal-length cables. Similarly, the ECL

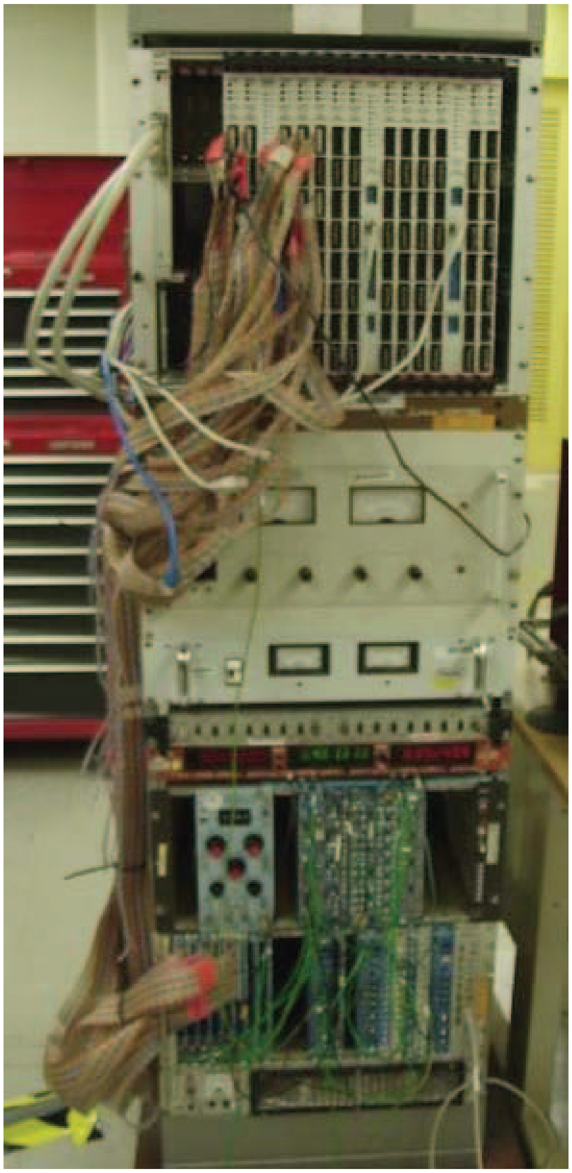

Fig. 6. Photograph of the trigger system at Argonne National Lab.

outputs are connected to the I/O cards of the Topological Trigger using equal-length ribbon cables.

Oscilloscope probing verifies that signals of 5 ns total pulse width pass through the I/O cards, backplane and L1.5 cards without degradation. By moving the cables to the various inputs the connectivity of the system is exercised. This limitation was imposed by the availability of pattern generator modules; had sufficient number been available no moving of cables would be required. A test program written in National Instruments' LabWindows verified that the pixel mapping matched the VERITAS arrangement and that all crossover pixels were correctly routed. A photo of the test stand is given as Fig. 6.

The systemic delay of each pixel within the Topological Trigger crate is measured using a CAMAC TDC (LeCroy 2228, 50ps least count resolution). The common start of the TDC is a copy of the enable to the pattern generators. The multiplex output of each L1.5 trigger module is connected to one of the STOP inputs of the TDC. A 4GSamp digital oscilloscope was used to measure the propagation delay from the common enable signal to the assertion of each signal at the input of the I/O card and a table developed of the differences in assertion time for each pixel in the test stand. This is subtracted from the measured values to obtain the actual propagation delay for each pixel within the trigger system itself independent of the test stand.

A special variation of firmware was loaded into each L1.5 trigger module with minimal logic so that the FPGA acted as a simple 181-to-1 multiplexer allowing selection of any one input pixel (direct or crossover) to be re-driven to a front panel output with minimal variation in delay.

The Xilinx Virtex-5 FPGA used in the L1.5 contains programmable delay components on each input pin that provide 0-5 ns delay in steps of ~72ps. As each pixel is scanned the absolute delay is measured and then each pixel adjusted relative to the slowest. A typical result is shown in Fig. 7. The three L1.5 region processors are separated for clarity. The larger deviations at the right end of each L1.5 region's pixels are due to the longer backplane path lengths associated with crossover pixels between regions.

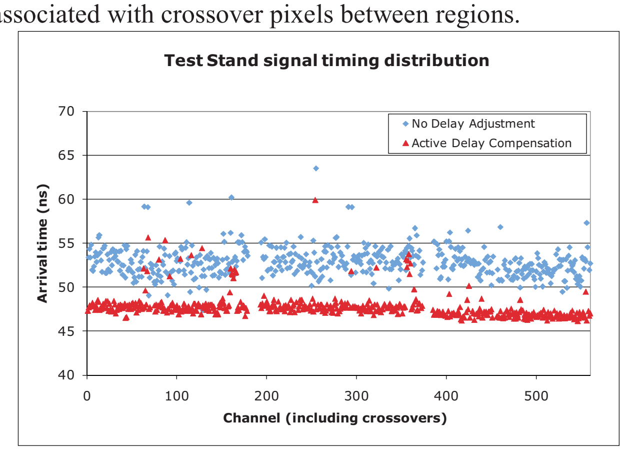

Fig. 7. Distribution of pixel propagation delays in the trigger system before and after timing compensation in the FPGA. Outliers in the adjusted delay values are still being investigated.

As a cross-check all I/O modules were cycled through one slot of the backplane to measure the variation in delay due to the parts in the I/O card. As Fig. 8 shows, the delay variance between I/O cards is minimal and the larger delay of crossover pixels is constantly repeated.

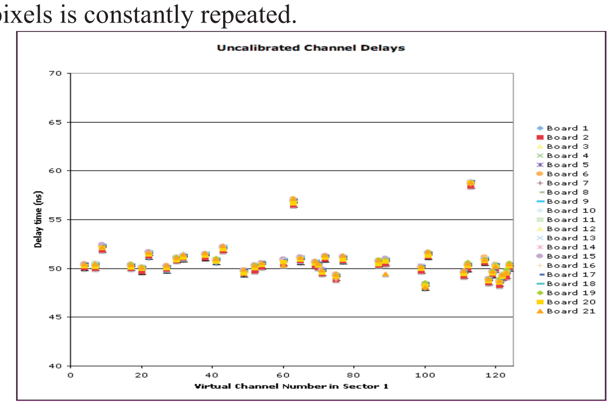

Fig. 8. Distribution of propagation delays of all I/O cards used in the same position. Outliers are crossover pixels.

IV. INSTALLATION AT THE VERITAS SITE

Field tests at the VERITAS site in Amado, AZ were performed in March of 2009. The purpose of the test was threefold:

1. To prove the operation of the trigger system in the field and demonstrate operation in parallel with and not affecting existing operations;
2. To compare the timing resolution and triggering efficiency to the existing trigger system;
3. To obtain measurements of the timing dispersion of the signals from the telescope and verify the increase in selectivity obtained by improved timing alignment of the input signals.

The VERITAS experiment consists of four IACT telescopes in an array, located at the Fred Lawrence Whipple Observatory (FLWO) in Amado, AZ. Fig. 9 shows a picture of the overall site.

Fig. 9. The VERITAS array at FLWO (picture courtesy of VERITAS).

Telescope T4 was chosen for the field test. The existing electronics of the telescope are mounted in three relay racks as shown in Fig. 10. Two outer racks, each containing two crates of discriminator/FADC modules, flank a center rack holding support electronics and the existing telescope trigger.

Fig. 10. Existing discriminator/trigger electronics at telescope T4.

The initial stage of the test was to unpack and install our electronics into spare relay rack space near the existing electronics. A set of 50 ribbon cables (20 pixels per each pair of cables) were labeled and run under the floor. For every set of pixels, the existing cable from discriminator to trigger was removed and two cables added – one from discriminator to the new pattern trigger and one from the new pattern trigger back to the old trigger as shown in Fig. 11. The termination of the differential ECL signals in the existing system is located at the old trigger, so the high input impedance of the I/O cards of the topological trigger does not affect signal quality. A measurement of the different signal delay of the new cable plant was made and a compensatory change to the look-back time for the experiment's existing trigger was made so that FADC data would have the same relative delay as when the shorter cables were in place.

Fig. 11. The fast pattern trigger installed in the trailer at telescope T4.

V. TEST RESULTS

The first exercise was to determine that the system was wired correctly and that VERITAS operations were unaffected by the new cable plant. Diagnostic registers in the L1.5 board allow for asynchronous sampling of the pixel values and internal FIFOs allow for capture of very short records of pixel activity. By using these in conjunction with the telescope's laser pulser system that illuminates all pixels and adjustment of discriminator thresholds, the entire cable plant may be verified. By doing so we determined that every pixel was correctly connected to the new pattern trigger and also that the pixels were still all correctly wired to the old trigger. This test additionally located 20 malfunctioning discriminator outputs that the experiment was unaware of, proving once again the value of built-in diagnostics at all layers of hardware.

Once connectivity was established and verified the experiment performed a full night of observations with the topological trigger in place. As expected no ill effects were recorded. During this experimental run the new trigger was configured with the external TDC to set up for delay compensation measurements.

The following evening, prior to observation time, the telescope's laser pulser system was used to illuminate all pixels at the same time. Each pixel in turn was routed by firmware to the TDC and the delay of each measured. Compensatory delays were then programmed into the L1.5 cards and the measurements repeated. As shown in Fig. 12, the full-width half-max spread of the distribution was reduced from 3.3 ns to 1.5 ns over the entire face of the telescope.

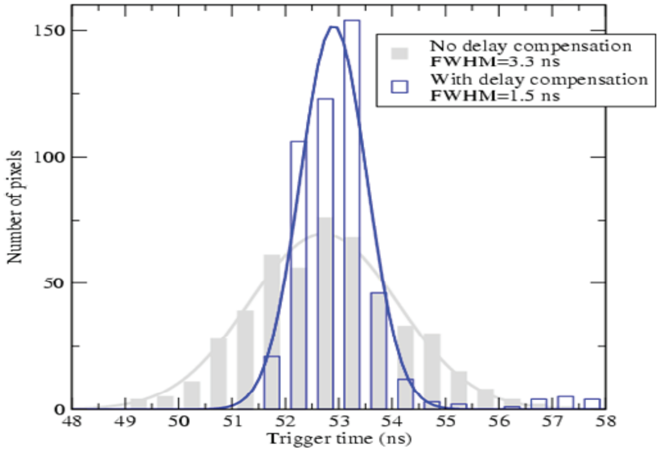

Fig. 12. Reduction in spread of pixel bit arrival times after application of delay compensation in L1.5 region processor boards.

The ability of the system to compensate for delay variation was limited by the maximum delay adjustment possible within the firmware. The L1.5 delay adjustment is implemented within the Virtex-5 FPGA and uses a single IDELAY element on each input that has a maximum compensation of 5 ns. We are investigating methods to extend the range of the delay adjustment with the goal of achieving a FWHM of 0.5 ns in the production version of the system.

Efficiency of the topological trigger was verified by selecting sets of three pixels with well matched arrival times and then adding cable delays to just one of them to "sweep" the one pixel past the coincidence of the other two. The L1.5 firmware uses sampling at 2.5 ns and an internal digital monostable fired by the leading edge of the input signal to insure that the internal signal used in the coincidence logic is always 5 ns long. We therefore expect that the topological trigger should be 100% efficient over a 5 ns window with linearly decreasing efficiency over a 2.5 ns range at either end of the window. As shown in Fig. 13, this is exactly what is measured.

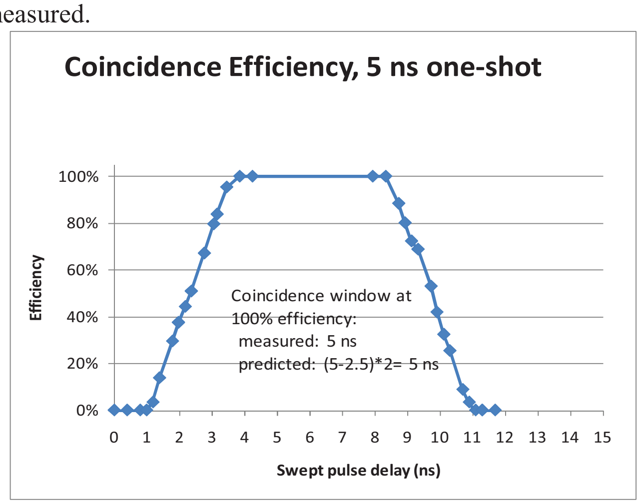

Fig. 13. Coincidence efficiency of L1.5 logic sweeping one pixel in time across the coincidence of two other pixels.

Similar measurements done previously by VERITAS staff indicate that the timing window of the existing trigger system in telescope T4 is wider (approximately 8-9ns). Verbal information provided by VERITAS indicates that the coincidence resolution of each telescope is slightly different as the existing trigger is not a synchronous sampling design.

Upon completing the adjustment of the timing compensation direct comparison of the performance of the topological trigger relative to the old trigger could proceed. This is accomplished by sweeping the threshold setting of the discriminators over a range of settings and measuring the rate at which each trigger system fires. At low thresholds the system is swamped by random events caused by night sky background. As the threshold is increased the trigger rate decreases but at some point the curve has a inflection point where the night sky background rate becomes small relative to the rate of real triggers due to gamma or cosmic ray events. Lowering the threshold setting at which this inflection point occurs is desired as this allows study of a wider range of energies.

Fig. 14 shows the result of this comparison. The bias curve obtained for the existing VERITAS system matches that obtained when the topological trigger system is not present. The narrower coincidence width of the topological trigger provides a lower inflection point due to better suppression of night sky background. In addition, a somewhat higher cosmic ray trigger rate was observed. We attribute this in part to the topological trigger having a slightly larger field of view than the old trigger, as it was discovered during the field test that the old trigger does not connect to a few of the pixels at the outer edge of the telescope. The majority of this increase is attributed to increased efficiencies obtained from the better timing alignment of the pixels in the new system.

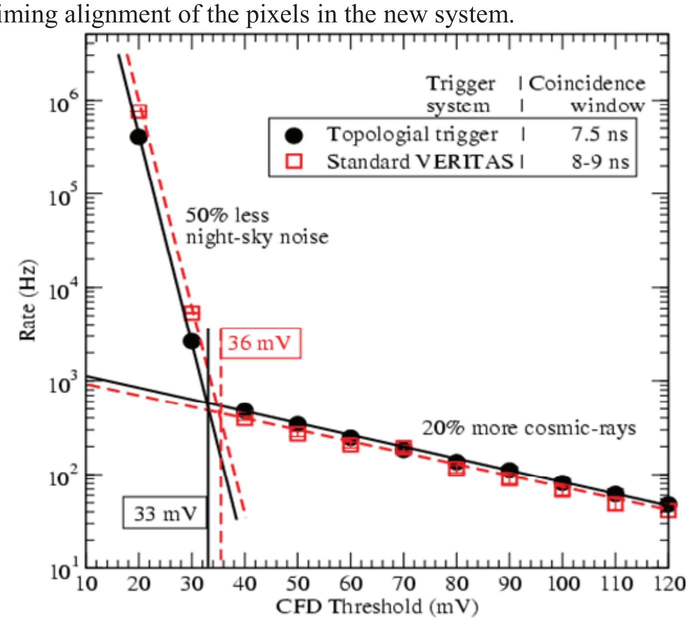

Fig. 14. Bias curve obtained from simultaneous observation with topological trigger and old trigger. The topological trigger provides a measurable improvement in performance allowing for lower threshold settings.

VI. PLANS FOR FUTURE WORK

Based upon the field test results the VERITAS Executive Board has included the Iowa State-Argonne fast pattern recognition trigger as one of the major components in the upgrade proposal submitted to the funding agencies. While waiting upon the results of these proposals we continue to finish the development of the system, specifically the L2 – L4 fiber optic data transmission and exercising the L1.5-to-L2 data transmission and event building under conditions of high background. We are actively engaged in discussion with other IACT experimental groups such as AGIS. We intend to manufacture sufficient hardware to instrument all four telescopes at VERITAS including implementation of the parallaxwidth trigger and look forward to reporting these results at a future conference.

VII. SUMMARY

We have designed and manufactured a very fast pattern recognition trigger for use in ground based gamma ray telescope arrays. The design is well advanced and modular so is applicable to future experiments in the field. A successful field test of the system was performed at the VERITAS site, implementing one telescope of the array. Work is in progress towards construction of a multi-telescope system and production of sufficient hardware to implement a four-telescope array will begin soon.

ACKNOWLEDGMENT

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